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APPLICATION N	0.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/081,624		02/20/2002	Jason L. Fuller	108298636US	1950	
25096	759	0 10/12/2005		EXAMINER		
PERKIN	S COI	E LLP	HARAN, JOHN T			
PATENT-	-SEA	•				
P.O. BOX	1247			ART UNIT	PAPER NUMBER	
SEATTLE	E, WA	98111-1247	1733			
				DATE MAILED: 10/12/2005		

Please find below and/or attached an Office communication concerning this application or proceeding.

				40.				
		Application No.	Applicant(s)					
		10/081,624	FULLER ET AL.					
	Office Action Summary	Examiner	Art Unit	-				
		John T. Haran	1733					
Period fo	The MAILING DATE of this communication app or Reply	ears on the cover sheet with the c	orrespondence address					
WHIC - Exter after - If NO - Failu Any r	ORTENED STATUTORY PERIOD FOR REPLY CHEVER IS LONGER, FROM THE MAILING DANSIONS of time may be available under the provisions of 37 CFR 1.13 SIX (6) MONTHS from the mailing date of this communication. period for reply is specified above, the maximum statutory period were to reply within the set or extended period for reply will, by statute, reply received by the Office later than three months after the mailing ed patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATION 36(a). In no event, however, may a reply be tim vill apply and will expire SIX (6) MONTHS from 1, cause the application to become ABANDONE	N. lety filed the mailing date of this communication. O (35 U.S.C. § 133).					
Status			•					
1)⊠	Responsive to communication(s) filed on 19 Se	eptember 2005.						
·	This action is FINAL . 2b) This action is non-final.							
3)□	Since this application is in condition for allowance except for formal matters, prosecution as to the ments is							
	closed in accordance with the practice under E	Ex parte Quayle, 1935 C.D. 11, 45	53 O.G. 213.					
Dispositi	ion of Claims							
4)⊠	Claim(s) <u>1,2,8-11 and 48-53</u> is/are pending in t	the application.						
	4a) Of the above claim(s) is/are withdrawn from consideration.							
5)	Claim(s) is/are allowed.							
6)⊠	Claim(s) <u>1,2,8-11 and 48-53</u> is/are rejected.							
-	Claim(s) is/are objected to.							
8)[_]	Claim(s) are subject to restriction and/o	r election requirement.						
Applicati	ion Papers							
9)	The specification is objected to by the Examine	r.						
10)	The drawing(s) filed on is/are: a)☐ acco	epted or b) \square objected to by the E	Examiner.					
	Applicant may not request that any objection to the	drawing(s) be held in abeyance. See	e 37 CFR 1.85(a).					
_	Replacement drawing sheet(s) including the correct		•					
11)	The oath or declaration is objected to by the Ex	aminer. Note the attached Office	Action or form PTO-152.					
Priority u	ınder 35 U.S.C. § 119							
_	Acknowledgment is made of a claim for foreign All b) Some * c) None of:		-(d) or (f).					
	1. Certified copies of the priority documents		N-					
	2. Certified copies of the priority documents3. Copies of the certified copies of the priority							
	application from the International Bureau	•	d in this National Stage					
* 5	See the attached detailed Office action for a list		ed.					
			·					
Attachmen	t(s)							
1) Notic	e of References Cited (PTO-892)	4) Interview Summary						
3) 🔲 Inforr	e of Draftsperson's Patent Drawing Review (PTO-948) mation Disclosure Statement(s) (PTO-1449 or PTO/SB/08) r No(s)/Mail Date	Paper No(s)/Mail Da 5) Notice of Informal P 6) Other:	ate atent Application (PTO-152)					

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DETAILED ACTION

1. This office action is in response to the amendments and arguments filed on 9/19/05.

Affidavit

2. The declarations filed on 2/18/05 and 9/19/05 under 37 CFR 1.131 are sufficient to overcome the Tandy (U.S. Patent 6,212,767) reference. All are rejections involving Tandy are hereby withdrawn.

The declaration filed on 2/18/05 provides conception of the claimed subject matter prior to the 102(a) date of Tandy (4/10/01) and the declaration filed on 9/19/05 demonstrates diligence from the date of conception to the date of filing.

It is noted that Tandy is not available as art under 102(e) as common ownership was properly asserted in the response filed on 10/6/04.

It is also noted that item 3 of the declaration filed on 9/19/05 has a typo in that the date should have been 3/26/01 and not 3/26/03.

Claim Rejections - 35 USC § 103

- 3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

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4. Claims 1, 2, 8-11, and 48-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Lim et al (U.S. Patent 6,378,200) and Leonard (U.S. Patent 6,071,371).

The admitted prior art is directed to a method for assembling microelectronic dies wherein a flip chip die is mounted on a substrate with a first die attach machine; then the flip chip/substrate subassembly is heated to reflow solder bumps to attach the flip chip to the substrate; then the flip chip/substrate subassembly is transported to a second die attach machine for dispensing epoxy on the backside of the flip chip and mounting a wire bond chip to the epoxy; and then heating the stacked die assembly to cure the epoxy (Specification 0005) Additionally the process can be performed by using a single die attach machine and running the substrate through it twice, once to attach the flip chip and once to attach the wire bond chip (Specification 0006). The admitted prior art is silent towards using a single heating cycle to secure both the flip chip to the substrate and the wire bond chip to the flip chip and towards having a single die attach machine with first and second die attach heads wherein the substrate is moved from one die attach head to another.

It is generally well known and conventional in the assembly art when assembling a plurality of chips to a substrate to have a single die attach machine with a plurality of stations, each station with its own die attach head (pick and place tool), wherein at each station particular types of chips are applied to the substrate, the substrate is moved to the next station where different types of chips are applied to the substrate and after all the chips are mounted on the substrate, the substrate is moved to a heating means for

heating the attachment means between the chips and substrates to securely attach the chips to the substrate, as shown for example in Lim et al (See Figure 1; Column 2, line 39 to Column 3, line 50). One skilled in the art would have readily appreciated the advantages of such a system over the method of the admitted prior art because it provides for one heating step rather than multiple thereby increasing the efficiency as further evidenced by Leonard et al.

Leonard et al is directed towards a method for bonding two dies to a circuit board, one via solder and the other via curable adhesive and teaches that it is preferable to perform one heating cycle to both reflow the solder and cure the adhesive rather than two separate heating cycles, one for the solder and one for the adhesive, because the additional heating has detrimental effects and is inefficient (Column 1, line 40 to Column 2, line 40).

One skilled in the art would have readily appreciated that the collective teachings of Lim et al and Leonard et al point out the inefficiencies of the admitted prior art and suggest modifying the method of the admitted prior art to have a single die attach machine with two die attach stations, each with its own die attach head, wherein the flip chip is mounted on the substrate at the first station by a first die attach head, is transported directly to a second station wherein the wire bond chip is mounted on the flip chip by a second die attach head and then the entire assembly is transported to a heating means for heating the solder and adhesive simultaneously in a single heating cycle to attach the flip chip to the substrate and the wire bond chip to the flip chip. Such

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a method would have increased efficiency and productivity as suggested in Lim et al and Leonard et al.

Regarding claims 1, 2, 8-11, and 48-53 it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of the admitted prior art as suggested above by the collective teachings of Lim et al and Leonard et al in order to increase the efficiency and productivity of the admitted prior art.

Response to Arguments

5. Applicant's arguments filed 9/19/05 have been fully considered but they are not persuasive.

The above rejection was made in the previous office action mailed 4/20/05 (see Paragraph 6) and was not addressed in the response filed 9/19/05. This rejection did not rely upon Tandy and the response only argued the rejection involving Tandy.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

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mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

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7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John T. Haran whose telephone number is (571) 272-1217. The examiner can normally be reached on M-Th (8 - 5) and alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Dunn can be reached on (571) 272-1171. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John T. Haran Primary Examiner

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